23. (New) The processor of claim 1, wherein the register specifier is encoded as an indirect specifier.

REMARKS

Claims 1, 3-17 and 19-22 are rejected under 35 USC 103(a) as being unpatentable over Baxter (U.S. Patent No., 5,826,096) in view of Jouppi (U.S. Patent No. 5,150,469). Applicants respectfully traverse these rejections.

In response to Applicants' argument distinguishing claim 1 from the cited reference, Examiner stated that there is no recitation in the claims as to whether the implicitly derived register is for a next, current or past instruction. Claim 1 is amended to clarify that the instruction operates on at least two registers including at least one register explicitly identified by a register specifier and at least one other register implicitly identified by the register specifier.

Further, Applicants amended claim 20 in the previous response to clarify that both the explicitly identified register and implicitly identified registers are operated upon during executing of the instruction. Accordingly, amended claim 1 and claim 20 are patentably distinguishable from the cited reference. Applicants respectfully submit that amended claim 1 and claim 20 and those depend therefrom are in condition for allowance.

Further, in rejecting claims 3-17, 19 and 21-22, citing Rule 1.111(c), Examiner stated that Applicants fail to point out the patentable novelty presented in claims 3-17, 19 and 21-22. Applicants would like to respectfully point out that Rule 1.111(c) refers to Applicants' response in lieu of claims amendment however, in their response, Applicants did not amend claims 3-17, 19 and 21-22. In the previous office action, claims 3-17, 19 and 21-22 were generally rejected in view of the cited references. Examiner did not specifically point out the relevant teaching of the cited reference relied upon with reference to the relevant sections. In their response, Applicants requested Examiner to specifically point to the sections of the cited references on which the elements of the claims read upon. In rejecting claims under 35 U.S.C. 103(a), the Examiner must establish a prima facie case of obviousness. "[T]he examiner should set forth in the Office action: (A) the relevant teaching of the prior art relied upon, preferably with reference to the

relevant column or page number(s) and line number(s) where appropriate ...." *See* MPEP §706.02(j). Applicants are entitled to a substantive examination of the presented claims and respectfully request Examiner to withdraw the finality of the rejection or in alternative, issue a notice of allowance.

Examiner has stated that Applicants fail to point out the claimed decoder in the drawings to show how the decoder is able to "implicitly deriving said implicitly derived register...." The issue of decoder function was not raised by the Examiner in the previous office action however, Applicants addressed this issue in a paper submitted on October 19, 2000 which was in response to an office action dated July 20, 2000, the details of which are incorporated herein by reference thereto. Further, the issue was discussed and resolved with Examiner during a telephonic interview on March 2, 2001, the details which are incorporated herein by reference thereto. Accordingly, Applicants respectfully submit that claims 1, 3-17 and 19-22 are in condition for allowance.

Applicants respectfully request Examiner for a telephonic interview to discuss the relevant issues for disposal and if necessary, clarification for appeal.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Abdul R. Zindani — 1-31-03 (Date)

Respectfully submitted,

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PATENT

MARKED-UP COPY OF MARKED-UP COPY OF AMENDED CLAIMS IN ACCORDANCE WITH 37 C.F.R. § 121(c)(ii)

1. A processor comprising:

a register file **[including a plurality *of* registers]**; **and**

a functional unit, coupled to the register file, **that executes [executing]** an instruction **that [operating] operates** upon **plural registers of** said **[plurality *of* registers in the]** register file, **including at least one register explicitly identified by a register specifier and at least one other register implicitly identified by the register specifier. [the instruction in which a register specifier is implicitly derived, based on an explicitly-specified register specifier; and**

a decoder coupled to the functional unit and coupled to the register file, the decoder implicitly deriving said implicitly derived register specifier based on said explicitly-specified register specifier *of* the instruction.]